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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
02/05/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/043,276	NAKATANI ET AL.	
	Examiner	Art Unit	
	JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) *4-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6410414) in view of Toyosawa et al. (US 6441467), hereinafter Toyosawa.

Regarding claim 1, Fig. 6 of Lee shows semiconductor device comprising:

a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor device is formed (100; active region; col.3, lines 5-10);

an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and

a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a Surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold and a projection area of the metal interconnect layer connected with a bonding wire is overlapped with said functional semiconductor device. Fig. 1 of Toyosawa shows said metal interconnect layer (17) being consist of gold material; and a projected area of the metal interconnect layer connected to a bond wire (col. 3, lines 20-27) is overlapped with the functional semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Toyosawa in order to have the top metal interconnect layer consisting of gold to increases the conductivity and mechanical strength of the interconnection layer, and to have a bond wire connected to the region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires.

Regarding claim 3, Toyosawa discloses that the insulating layers are deposited by plasma CVD method (col. 7, lines 13-18). In addition, “high-density plasma CVD” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, Fig. 6 of Lee shows semiconductor device comprising:

a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor region is formed (100);

an inter layer dielectric (104) directly covering a portion of top surface and the side surfaces of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and

a planarized polyimide (116; col. 5, lines 47-52) which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and an interconnection (114) is connected to the region of the metal interconnect layer.

Fig. 6 of Lee shows substantially the entire claimed structure except the metal interconnect layer (the uppermost metal layer) made of gold, a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region and a projection area of the metal interconnect layer connected with a bonding wire is overlapped with said functional semiconductor device. Fig. 1 of Toyosawa shows said metal interconnect layer (17) being consist of gold material, a barrier layer (16) covering the contacting hole and a portion of a surface of the interlayer insulating film (10) around the contacting hole, thereby forming a barrier layer region, and a projected area of the metal interconnect layer connected to a bond wire (col. 3, lines 20-27) is overlapped with the functional semiconductor device. It would have been obvious to one of ordinary skill in the art at

the time of the invention to incorporate the teachings of Toyosawa in order to have the top metal interconnect layer consisting of gold to increases the conductivity and mechanical strength of the interconnection layer, and to have a barrier layer region for improved conductivity, and further to have a bond wire connected to the region of the metal interconnect layer to accommodate the connection of the functional semiconductor device with wires.

Regarding claim 9, Toyosawa disclose that the barrier layer consists of titanium (col. 7, lines 48-50).

Regarding claims 10 and 11, Harada discloses the first interconnect layer consists of aluminum (col. 24, lines 31-32).

Regarding claim 12, Harada discloses the inter layer dielectric consists of USG film (201b, siliconoxide; col. 13, lines 52-55).

Regarding claim 13, Fig. 1 of Toyosawa shows the functional semiconductor region further comprises a polysilicon gate (3) isolated from the first interconnect layer by a second dielectric layer (10), wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer. Toyosawa disclose that the barrier layer consists of titanium (col. 7, lines 48-50).

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the 88examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Junghwa M. Im/
Examiner, Art Unit 2811

/J. M. I./
Examiner, Art Unit 2811